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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,894	03/26/2004	Tomohiko Koto	108075-00126	7803

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,894	KOTO, TOMOHIKO	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-14* is/are allowed.

6)☒ Claim(s) *2-4,6,7,15,16 and 18-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-4, 6, 15, 16, and 18-20 are rejected under 103(a) as being unpatentable over Dillon (U. S. PAT. 6,590,422) in view of Hayashi et al. (U.S. 6,774,695).

In claim 2, Dillon teaches all claimed features in Fig. 2 a semiconductor integrated circuit comprising: a level conversion circuit (140) having a pair of transistors including a first MOS transistor (31) and a second MOS transistor (33A), connected in series between a first power supply (VDD) and a second power supply (Ground), and a further pair of transistors including a third MOS transistor (32A) and a fourth MOS transistor (34A), connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node (a node between 31A and 33A) connecting the first and second MOS transistors and a second output signal from a node (a node between 32A and 34A) connecting the third and fourth transistors; and a differential amplification circuit (26), connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit, wherein the first and fourth MOS transistors each have a gate for receiving a first input signal (one of differential signals 52), and the second and third MOS transistors each have a gate for receiving a second input signal having a

phase inverted from the phase of the first input signal (the other one of differential signals 52); with the exception of teaching wherein the gate of each transistor has a gate length and a gate width. However, Hayashi et al. teaches in col. 3, lines 32-45, the gate of each transistor has a gate length and a gate width (property of each transistor), the ratio between the gate length and the gate width of one of the transistors in each pair of the series transistors is about three time or less than the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors (the ratio between the gate width and the gate length of the first p-channel type MOS transistor may be set to be greater than the ratio between...)

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to have combined the teachings of Dillon with the teachings of Hayashi for reducing the on-resistances of the first p-channel MOS transistor and the second n-channel MOS transistor, contributing to further accelerating the variation of the output signal.

In claim 3, Dillon further teaches the semiconductor integrated circuit according to claim 2, wherein gate of each transistor has a gate length and a gate width (property of each transistor), and the ratio between the gate length and the gate width of one the transistors in each pair of the series-connected MOS transistors substantially the same as the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors (since Dillon does not talk about any differences in the ratio between the gate length and the gate width of one

the transistors in each pair; the ratio between the gate length and the gate width of one the transistors in each pair must be the same).

In claim 4, Dillon further teaches the semiconductor integrated circuit according to claim 2, wherein each transistor has a gain constant (property of each transistor), the gain constant of one of the transistors each pair of series-connected MOS transistors substantially the same constant of the other one of the transistors of the series-connected MOS transistors (since Dillon does not talk about any differences in the gain constant of one the transistors in each pair; the gain constant of one the transistors in each pair must be the same).

In claim 6, Dillon further teaches the semiconductor integrated circuit according to claim 2, wherein the differential amplification circuit (26) is connected between the first power supply (VDD) and the second power supply (ground).

Claims 15 and 16 correspond to detailed circuitry already discussed similarly with regard to claims 2.

Claim 18 corresponds to detailed circuitry already discussed similarly with regard to claims 2.

Claims 19 and 20 correspond to detailed circuitry already discussed similarly with regard to claims 3 and 4.

3. Claim 7 is rejected under 103(a) as being unpatentable over Dillon (U. S. PAT. 6,590,422) in view of Tinsley (US 2003/0085736).

In claim 7, Dillon teaches all claimed features in Fig. 2 a semiconductor integrated circuit comprising: a level conversion circuit (140) having a pair of transistors

including a first MOS transistor (31) and a second MOS transistor (33A), connected in series between a first power supply (VDD) and a second power supply (Ground), and a further pair of transistors including a third MOS transistor (32A) and a fourth MOS transistor (34A), connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node (a node between 31A and 33A) connecting the first and second MOS transistors and a second output signal from a node (a node between 32A and 34A) connecting the third and fourth transistors; and a differential amplification circuit (26), connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit, wherein the first and fourth MOS transistors each have a gate for receiving a first input signal (one of differential signals 52), and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal (the other one of differential signals 52); with the exception of teaching wherein the first to fourth MOS transistors each include a source and a back gate, which is connected to the source. However, Tinsley et al. teaches in Fig. 5, the first to fourth MOS transistors each include a source and a back gate, which is connected to the source.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to connect back gate to source for first to fourth transistors, as taught by Tinsley et al. to reduce body effect of each transistor, thus allowing the circuit to operate at high speed.

4. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 8-14 appear to comprise allowable subject matter(s).

Response to Arguments

6. Applicant's arguments with respect to claims 2, 7, 15 and 18 have been considered but are moot in view of the new ground(s) of rejection.

The new ground of rejection(s) has been set forth as discussed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER